Nanotechnology Development for CMOS Image Sensor Applications

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ABSTRACT

Pixel size scaling is a development trend in CMOS Image Sensor (CIS) to achieve high array resolution and chip miniaturization for lower cost and smaller device form factors. The latter is especially important for mobile smart handset market. Technology challenges arise due to the scaling for maintaining optical and electrical pixel performance. The limited pixel size constraints the in-pixel transistor dimension and the noise performance at signal readout is thus degraded. Nanotechnologies were utilized in different aspects of CIS development to mitigate the shortcomings caused by pixel scaling. Among them, backside illumination (BSI) technology, pixel-to-pixel isolation technique, optical thin film control, micro-lens/color filter shift, and in-pixel device noise reduction technique are described in this paper.

NANO TECHNOLOGY BREAKTHROUGHS FOR CIS

A CIS chip typically contains a pixel sensor array and a set of periphery readout circuitry, as the schematic shown in Fig. 1. The following sections describe technical breakthroughs to allow pixel size shrunk down to 1.4μm or even sub-micron (~0.9μm) scale.

(1). Backside illumination (BSI) technology vs. traditional front-side illumination (FSI) technology:

For traditional FSI structure, pixel shrinkage induces optical performance degradation, such as lower quantum efficiency (QE), higher cross-talk between pixels, and worse angular response, due to optical blockage and interference effect from metal routing layers. A BSI structure, nominally with 100% fill factor, was developed to avoid the physical barrier by relocating metal layers away from the optical path (as shown in Fig. 2) [1] BSI technology involves several technical advancement including wafer bonding, wafer thin-down with precise thickness control, fine passivation of backside Si surface, and so on. This disruptive technology has been adopted by CIS manufacturers for high-end mobile imaging devices.

(2). Pixel-to-pixel isolation:

A CIS sensor array relies on an effective pixel-to-pixel isolation structure to avoid carriers at a specific pixel to leak to adjacent pixels (so-called cross-talk). A typical approach is to build up an electrical barrier by a p-n junction with certain depth between photodiodes (PDs) using ion implantation of reverse-type dopant surrounding PDs. As pixel size scales down, the aspect ratio of the implantation masking layer needs to be increases to avoid squeezing the PDs. For a pixel size on the order of 1μm, the required aspect ratio of the implant masking layer is typically 15-20 (as shown in Fig. 3). Special hard mask approach was developed to achieve the required aspect ratio. Figure 4 shows quantum efficiency of 1.1μm pixels with BSI Si thickness 2.0 and 2.3μm respectively by different isolation schemes. The one with thicker Si thickness demonstrates better QE at green and red wavelengths due to higher absorption in Si.

Some other approach implements deep trench isolation structure with proper gap filling materials [2, 3]. Applying the same concept, the aspect ratio of the etching masking layer is also high and requires special hard masking technique for implementation.

(3). Micro-lens/Color Filter Array (CFA) shift and optical film thickness control:

The optical incident angle to a pixel, as its location not at array center, is generally not zero. With a small pixel size, the micro-lens and CFA above the pixels need to be shifted to accommodate the incident angle of the optical rays to avoid optical crosstalk, as shown in Fig. 5. The shift is generally done by mask design and requires precise process control on the order of several tens to one hundred nm of overlay.

The optical film thickness control, both within-wafer and wafer-to-wafer control, is as important for CIS QE uniformity. Figure 6 shows QE of the sensors from wafer center / edge with ~30nm film thickness deviation in one layer of the film stack. The QE curves show obvious discrepancy and affect sensor’s color fidelity. Study of the optical film thickness control involves optical simulation to achieve an optically robust film stack design for manufacturing.

(4). Low-noise device development:

As pixel size shrinks, the allowed device dimension inside a pixel for signal readout is also reduced. Noise associated with the source follower amplifier transistor also increases, which becomes a performance bottleneck. Literature study [4] shows that major noise source comes from trap states at gate oxide interface and shallow trench isolation (STI) edge. To overcome this shortcoming, a self-aligned junction isolation (SAJI) transistor structure with buried channel (BC) implant was proposed [5]. The top-view and cross-section of the device are drawn in Fig. 7. The spectral noise power density of the proposed SAJI-BC device, as compared with a typical STI-SC device, is shown in Fig. 8. One to two orders of magnitude of noise spectral density improvement was observed from the SAJI-BC device. The noise of small transistor is improved by the structure.

SUMMARY

Modern nanotechnologies were utilized in CIS applications to maintain pixel performance while reducing pixel sizes. BSI technology, pixel isolation technique, micro-lens/CFA shift control, and new low-noise device implementation are among the significant examples. As the pixel scaling trend continues, more nanotechnology development in this field would be required to maintain the momentum of technology advancement.

REFERENCE

Figure 1. The schematic of typical CIS chips. It generally contains a pixel array and periphery circuits for signal readout.

Figure 2. Traditional FSI structure (left) vs. newly developed BSI structure (right). Breakthroughs in manufacturing technology have been developed as described in the paper.

Figure 3. A special implant masking technology with high aspect ratio (~15-20) is developed for good pixel-to-pixel isolation.

Figure 4. QE spectrum of 1.1μm pixel array with BSI Si thickness 2.0μm and 2.3μm. The curve with thicker Si shows higher QE.

Figure 5. Micro-lens / color filter shift with precise location control needs to be implemented on CIS device for optimized optical performance (e.g. QE and cross-talk).

Figure 6. QE difference due to optical film thickness variation for die location at wafer center and wafer edge.
Figure 7. Top view and cross-section of the proposed SAJI-BC device structure.

Figure 8. Comparison of device noise power spectral density for the proposed SAJI-BC device and a typical STI-SC device. The SAJI-BC shows more 1-2 orders better noise performance.