High Performance Conducting Bridge Resistive Memory Featuring a Novel Reliable Structure (Invited)

Macronix Emerging Central Lab., Macronix International Co., Ltd.
16 Li-Hsin Rd. Hsinchu Science Park, Hsinchu, Taiwan, ROC

TEL: +886-3-5786688 ext 78158, FAX: +886-3-5789087, Email: FMLee@mxic.com.tw

Abstract

A novel solid-electrolyte based electrochemical induced conducting bridge (CB) resistive memory (ReRAM) is proposed to solve two key reliability issues. The first issue is regarding to the poor data retention and cycling endurance from the unstable conducting bridge. The second issue comes from the degradation of the dielectric layer caused by the high E-field just before the filament is completed (or begins to disrupt) during memory operations. The proposed new device consists of an additional p-type CuO layer between the Cu-ion supply layer and the dielectric, which acts both the E-field moderator as well as the Cu back-diffusion barrier and greatly increases the reliability of the device. Much of this report has been published in the 2013 Symposium for VLSI Technology [1], and selected as one of the highlight papers. Here, we report the same results as an invited paper.

Introduction

Conducting bridge ReRAM has drawn much interest recently because of its high On/Off ratio, high speed, and good scalability [2]. The typical Cu-based resistance switching characteristics (Fig. 1a) are carried out by electrolytic reactions that SET (form) or RESET (rupture) the conduction filament (CF) in the SiO2 layer (Fig.1b), denoted as the low resistance state (LRS) and the high resistance state (HRS), respectively. CB devices, however, often suffer from poor data retention and cycling endurance because the conducting bridge is feeble and unstable. In addition, as the SET/RESET cycling continues, the level of the SiO2 leakage current gradually increases due to the damage from the repeating high E-field stress inside the SiO2 layer. In this work, we propose a structure using a p-type CuO layer acting as the E-field moderating (EM) layer to reduce the SiO2 degradation. At the same time, it separates the Cu-ion source from the Cu conducting bridge and effectively prevents the back-diffusion (dissolution) of the Cu atoms from the bridge to the Cu source layer. With these two issues solved the reliability of the CB devices can be greatly improved.

P-type Semiconductor as a Buffer Layer and EM Layer

As a reference, the conventional SiO2/Cu-GST two-layer structure (Fig. 2(a) to (c)) was examined first. In LRS, by applying positive bias, a Cu conducting filament is formed but not stable. This is because the activation energy for Cu to form CuTe is low [3] thus Cu in the filament can easily dissolve into the Cu-GST (ion supply layer) at the interface. As a result a sudden jump in resistance from LRS to HRS can be found when the conducting bridge ruptures. In Fig. 2(d) to (f), a p-type CuO layer is inserted between the Cu filament in the SiO2 layer and the ion supply layer. The stability of the Cu filament is improved due to the low solubility of Cu atoms in the CuOx layer.

Figure 3 shows the defect/vacancy generation model in conventional CB device without the CuOx layer. The E-field in the gap between the growing CF and the top electrode (Cu-GST) can reach > 10MV/cm and generates defects and vacancies. Leakage paths can be formed through these defects and reduce the resistance of the HRS. The inserted p-type CuO layer can reduce the maximum E-field in the SiO2 layer and thus reduce the oxide damage issue.

Device Fabrication and Simulation Results

Figure 4 shows the TEM image of the device with reactively sputtered CuOx EM layer and its process flow. Figure 5 compares the E-field of the structures with and without EM at various SiO2 gap distance under different operation bias. As the filament grows and the SiO2 gap narrows, the EM dynamically controls the increase of the E-field in the SiO2 layer and reduces the voltage drop for up to 23%.

A wide range of variation on resistivity and hole concentration (obtained via Hall measurement) are achieved, as in Figs. 6(a) and (b). In addition, XRD and XPS spectra shown in Figs. 6(c) and (d) indicate the presence of CuO and Cu2O in the sputtered films.

Electrical Characteristics

Typical DC-sweep results for devices with and w/o the EM are shown in Fig. 7. For SET operation both devices switch from HRS to LRS at 0.75V. For RESET operation, however, device w/o the EM can only switch back to 10MΩ under negative bias, implying the existence of SiO2 leakage paths that limit the HRS level. The device with EM layer was cycled without any current limiter using 10µs SET/RESET pulses at 1.5V/-1.2V, as shown in Fig. 8. A 3-order resistance window was achieved with the endurance improved from 200K [4] to >1M cycles. Figure 9 shows the resistance distributions for devices with and w/o EM. The On/Off ratio was highly improved from 30X to ~ 1000X by the inserted EM layer. Excellent data retention performance for both RESET and SET states are shown in Fig. 10, where there is no resistance degradation during the 150°C, 240 hr bake. The CuOx layer not only reduces the maximum E-field during programming operations, but it also acts as a diffusion barrier that prevents the Cu atoms at the filament tip to back-diffuse into the Cu-GST layer [1].

Summary

A novel CMOS compatible electrochemical conducting bridge ReRAM cell structure is demonstrated. By inserting a p-type semiconductor layer (a CuOx layer) between the ion supplier and the memory layer the maximum E-field in the memory layer is drastically reduced. Not only an ultra-wide resistance window is obtained, this memory layer the maximum E-field during programming operations, but it also acts as a diffusion barrier that prevents the Cu atoms at the filament tip to back-diffuse into the Cu-GST layer [1].

References

Fig.1 (a) Typical resistance switching characteristics of the Conducting Bridge ReRAM. (b) Sketch of SET and RESET operation based on the electrochemical growth/disruption.

Fig.2 Schematic figures and retention behavior of two device types. The snapshots of structures w/o and w/ ion buffer layer are shown in (a, b, c) and (d, e, f), respectively. (a) and (d) represent the Cu path formed right after the set operation. In (b), the Cu atoms in the SiO$_2$ layer dissolve/diffuse into the Cu-GST layer. Finally, the Cu path breaks, as (c), and results in the retention failure. In Fig. 1(e), both the diffusivity and dissolution of Cu in SiO$_2$ and buffer layers are low and results in a stable Cu path, (f).

Fig.3 (a) Schematic of the time evolution for the CF growth. (b) As the growing filament approaches the Cu-GST layer, vacancies (Vo) are generated by the strong E-field inside the narrow SiO$_2$ gap.

Fig.4 TEM image and the cell structure of the EM Conducting Bridge device.

Fig.6 Ar/O$_2$ reactive sputtered CuO$_2$ films are analyzed: (a) Resistivity and (b) hole concentration by Hall measurement; (c) XRD and (d) XPS spectra. The resistivity decreases as O$_2$ ratio increases since the CuO is more conductive than Cu$_2$O. All samples show p-type behavior.

Fig.5 TCAD simulation of the E-field for various SiO$_2$ gap thickness under different operation bias. The EM helps to retard the rapid increase of the E-field in the SiO$_2$ layer by reducing the voltage for 23%.

Fig.7 DC I-V characteristics for the CB device with and without EM layer. The oxide leakage current is drastically reduced.

Fig.8 Pulse cycling test of the device with EM. ~3 orders of resistance window and over 1.4x10$^6$ cycles are achieved.

Fig.9 The resistance distribution for devices with and w/o EM. The resistance window increases from 30X to 1000X with the EM layer.

Fig.10 High temperature (150°C) baking test showing excellent data retention for both states.