Extraction of interfacial state density in high-k/III-V gate stacks: problems and solutions
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Group III-V semiconductor materials are expected to replace Si as a channel material in CMOS beyond the 11nm technology node (ITRS [1]). A highly disordered high-k/III-V interface presents one of the major concerns for the implementation of high mobility III-V surface channel MOSFETs. The transport properties of III-V channels were shown to significantly degrade near the interface with the gate oxide [2,3]. The interface trap density (D\textsubscript{it}) is an important figure of merit for the interface quality, which helps guiding the process improvement efforts. However, characterization of D\textsubscript{it} in the case of III-V channel is a challenging task: applicability of the standard D\textsubscript{it} extraction methods are diminished due to comparable values of the interface state density and density of carriers in the conduction band of III-V channel. This circumstance greatly complicates the determination of the real C\textsubscript{ox} value and separation of the true inversion response from that of the D\textsubscript{it}, i.e. establishing the E\textsubscript{F}—V\textsubscript{g} relation (see Fig. 1).

The reported D\textsubscript{it} values for the high-k/III-V stacks vary by the orders of magnitude (Fig. 2). To resolve the discrepancies, SEMATECH initiated the “golden wafer project” [4] focusing on identifying the best practice for the D\textsubscript{it} extraction, which could serve as an industry standard for benchmarking the gate stack D\textsubscript{it} data. In this project, the participating groups (SUNY Albany, TSMC, Intel, Global Foundry, IMEC, Georgia Tech, Penn State, UCSB, UCSD, NTU, Tyndall, Purdue, SEMATECH) performed the D\textsubscript{it} extraction using the capacitors fabricated on a single wafer (the golden wafer fabricated by SEMATECH). The variety of methods employed by different groups is discussed below. (i) Terman method [5] typically yields the highest D\textsubscript{it} values since slower traps can contribute to the carrier trapping process. The extracted D\textsubscript{it} value strongly depends on the assumptions used to calculate the ideal CV characteristic. (ii) In the High-Low frequency CV method, [6] the number of responding traps, and hence extracted D\textsubscript{it}, depends on the high and low frequency values and temperature. (iii) The conductance method [7] usually provides the lowest D\textsubscript{it} values because only the resonant traps respond can be accounted for. Similar to the conductance but a more rigorous equivalent admittance method [8] also yields D\textsubscript{it} in lower range of reported values.

To discuss the sources of discrepancies between the extracted trap densities we need to consider that the charge carriers at high-k/III-V interface can be captured not only by the interface states but also by the bulk oxide states/border traps as shown in the schematic of the traps distribution probed by admittance-based electrical characterization methods in Fig. 3. The characteristic time constant of the trapping/detraping processes depends on the trap energy, location, density of the available channel carriers and ambient temperature. Therefore, the extracted D\textsubscript{it} values reflect the contribution in the admittance from the interface and bulk/border traps. Thus, by using different frequencies and temperatures, the listed above methods probe different regions of traps spatial and energy distributions that may result in different D\textsubscript{it} values. However, even the same methods executed by different groups using the same experimental conditions may yield more than an order of magnitude mismatch in the D\textsubscript{it} values. Such large discrepancy cannot be explained by the device-to-device variability, but is found to be caused by differences in the C\textsubscript{ox} and N\textsubscript{d} parameters used in the D\textsubscript{it} extraction procedure.

In the generalized method proposed by SEMATECH, C\textsubscript{ox} and N\textsubscript{d} are extracted from the high-low frequency and Terman measurements simultaneously with the D\textsubscript{it} value. This method takes advantage of the finding that D\textsubscript{it} distributions extracted by the High-Low and Terman techniques exhibit different sensitivity to the variations in the C\textsubscript{ox} and N\textsubscript{d} values (Fig. 4). The iterative procedure uses the D\textsubscript{it} distribution vs. trap energy in the bandgap and C\textsubscript{ox} and N\textsubscript{d} as fitting parameters to reproduce experimental High and Low frequency C-V curves (Fig. 5). To reduce the interface trap response (excluding trap contribution to the measured capacitance), the high frequency C-V measurements are performed at low temperature while a low frequency C-V characteristic is measured at high temperature to activate as many traps as possible. Simulations of the ideal C-V curves are performed considering non-parabolic bands and multi-valley carrier distribution. Starting from the ideal C-V characteristic, the impact of traps is included as a “stretch-out” of the high frequency C-V curve, while in the simulated low frequency C-V an additional capacitance associated with the traps charging (C\textsubscript{trAPS}=qD\textsubscript{it}) is also taken into account along with the stretch-out effect. Fitting simultaneously both high and low C-V curves (Fig.6) allows the D\textsubscript{it} vs. E\textsubscript{F} to be determined and C\textsubscript{ox} (or EOT) to be extracted self-consistently. In the case of the golden wafer gate stack, 5nm ZrO\textsubscript{2}/1nm Al\textsubscript{2}O\textsubscript{3}/In\textsubscript{0.53}Ga\textsubscript{0.47}As, the high and low frequency C-V curves were measured at (1 MHz and 150 K) and (1 KHz and 375 K), respectively, and the extracted D\textsubscript{it} vs. E\textsubscript{F} distribution was of U-shape with a minimum density of ~ 9x10\textsuperscript{12} cm\textsuperscript{−2} eV\textsuperscript{−1} located -0.25 eV above the midgap (Fig. 7).

Frequency dispersion of the CV characteristics in accumulation (see Fig. 1) is associated with the presence of border traps in the high-k dielectric. The extracted D\textsubscript{it} includes also the border trap density projected to the substrate/dielectric interface. The spatial trap distribution through the oxide thickness can be extracted using the distributed capacitance method [9].

Minority carrier response is also taken into account while simulating the low-frequency CV curve. Neglecting the minority carrier response would have resulted in an overestimation of D\textsubscript{it} at the conduction band edge for the p-type samples. For the n-type samples, the contribution of the minority carriers to a low-f CV in the considered voltage range is small compared to the traps contribution.
Figure 1. Typical CV characteristics of the n-type 5nmZrO2/1nmAlO2/In0.53Ga0.47As MOS capacitor. (1) Low DOS in InGaAs and high Dit cause frequency dispersion of CV in accumulation (positive voltages) and complicate extraction of Cox value. (2) Frequency dispersion in negative voltages may be caused by both Dit and inversion carriers responses, which are difficult to separate.

Figure 2. Dit values at different energies in the InGaAs band gap as reported in the literature [8], [10]-[20]. (After [22]).

Figure 3. Schematic of the carrier trapping process at the interface, bulk and border traps in the gate stack.

Figure 4. (a) The relative error in extracted Dit values at midgap using Terman and high-Low techniques vs. error in assumed Tox (or Cox) values. (b) The fitting error of the high and low frequency CV curves fitting (see Fig. 6) vs. assumed EOT. The EOT value corresponding to the minimum fitting error represents the true EOT value.

Figure 5. Block-diagram of the SEMATECH method for self-consistent Dit and Cox extraction.

Figure 6. Fitting (blue solid lines) of the experimental high (black squares) and low (red circles) frequency CV curves of the In0.53Ga0.47As/2nm Al2O3/5nm ZrO2 (a) n-type (b) p-type sample. Fitting is obtained with the Dit distribution shown in Fig. 7.

Figure 7. Dit distribution extracted from n-type and p-type samples. Fig. 6.

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