High Mobility CMOS Technologies using III-V/Ge Channels
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CMOS utilizing high mobility III-V/Ge channels on Si substrates is expected to be one of promising devices for high performance and low power advanced LSIs in the future under sub 10 nm regime, because of the enhanced carrier transport properties [1-4]. Here, there can be several CMOS structures using III-V/Ge channels, as schematically shown in Fig. 1. While one of the ultimate CMOS structures can be the combination of III-V nMOSFETs and Ge pMOSFETs, viable CMOS structures using III-V and/or Ge channels are still strongly dependent on coming progress in the device/process/integration technologies of Ge/III-V n- and pMOSFETs.

Fig. 2 shows a variety of possible applications of III-V/Ge on the Si platform. In addition to the More Moore approach, this heterogeneous integration is expected to create novel LSIs or SoC utilizing a variety of device families along the More-than-Moore and the Beyond-CMOS approaches [3]. Here, MOSFETs using III-V/Ge must be fabricated on Si substrates in order to utilize Si CMOS platform, meaning the necessity of the co-integration of III-V/Ge on Si. However, there are still many technological issues to be solved for realizing this Ge/III-V-based CMOS on Si substrates such as (1) high quality Ge/III-V film formation on Si substrates (2) gate insulator formation with superior MOS/MIS interface quality (3) low resistivity source/drain (S/D) formation (4) total CMOS integration. In this paper, we address gate stack, channel and S/D engineering for improving the MOSFET performance with emphasis on thin EOT and ultrathin body, which are mandatory in the future nodes [3].

In this paper, we address gate stack and channel engineering for improving the channel mobility and the MOS interface properties with emphasis on thin EOT and ultrathin body, which are mandatory in the future nodes. As for Ge MOSFETs, we have proposed novel MOS interface control technology called plasma post oxidation, which can form GeOx/Ge interfaces beneath high-k films in order to realize thin EOT, low Dit and high mobility [5, 6]. By utilizing this technique, it is shown that HfO2/Al2O3/GeOx/Ge gate stacks have realized high quality Ge n- and p-MOSFETs with EOT of 0.76 nm. The hole mobility of 596 and 546 cm²/Vs and the electron mobility of 754 and 689 cm²/Vs have been obtained under...
EOT of 0.82 and 0.76 nm, respectively, for these Ge p- and nMOSFETs. The quite high mobility under very thin EOT is shown in Fig. 3 [4, 6].

As for III-V MOSFETs, direct wafer bonding technique is employed to form high quality III-V layers on Si substrates. We have demonstrated 3.5-nm-thick extremely-thin body InGaAs-OI MOSFETs on Si substrates with Al2O3 ultrathin BOX layers with high In0.53Ga0.47As/InAs thickness of 3 nm. Ni-InGaAs metal S/D technology allows us to realize low resistivity self-aligned S/D formation for ultrathin body InGaAs-OI MOSFETs [8]. Successful operation of 55 nm-channel length InGaAs/InAs/InGaAs-on-insulator MOSFETs have been demonstrated with superior short channel effect immunity (Fig. 4) [9]. The good performance is confirmed in Fig. 5. By utilizing these technologies, we have also demonstrated successful integration of InGaAs-OI nMOSFETs and Ge p-MOSFETs on a same wafer and their superior device performance [10].

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Figure 3 – The peak electron and hole mobility of the Ge p- and n-MOSFETs with HfO2/Al2O3/GeOx/Ge gate stacks vs. EOT, compared with the Ge MOSFETs with Al2O3/GeOx/Ge gate stacks and the data reported in other previous studies.

Figure 4 – Cross-sectional TEM images of the fabricated InAs-OI MOSFETs with Lch of 55 nm, Tbody of 3/3/3 nm.

Figure 5 – I_D-V_G characteristics of InAs-OI MOSFETs with Tbody of 3/3/3 nm, Tox = 6 nm. Good transfer and output characteristics were obtained due to thin channel thickness.